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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/601,204
Filing Date: June 20, 2003
Appellant(s): FAROOQUI, ARSHAD SUHAIL

Jason Paul DeMont
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 08/08/05 appealing from the Office action mailed 01/07/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Mosinskis et al.	USP 6529563	March 4, 2003
Connell et al.	USP 6441594	August 27, 2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 7, 8, 11 and 13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Mosinskis et al. (USP 6529653).

As to claim 7, Mosinskis et al. discloses in figure 3 an apparatus comprising: a bandgap reference voltage generator (360) having an output terminal; an operational amplifier (613) having a positive input terminal, a negative input terminal, an: an output terminal, wherein the positive input terminal of operational amplifier is electrically connected to the output terminal of the bandgap reference voltage generator *(noted that figure 3 shows the positive terminal of the amplifier 316 is coupled to the bandgap circuit. However, the negative terminal, instead of the positive terminal, of the amplifier must be coupled to the bandgap circuit in order to maintain the voltage at the drain of transistor M1 to be equal to the bandgap voltage)*; a transistor (M1) having a gate, a source, and a drain, wherein the gate of the transistor is electrically connected to the output of said operational amplifier, and wherein the drain of the transistor is electrically connected to the negative input terminal of said operational amplifier; and a voltage divider (R3, R4) having a input terminal, an output terminal, and a common terminal, wherein the input terminal of the voltage divider is electrically connected to the negative input terminal of the operational amplifier; a startup network (378, 374) having a positive supply terminal and an

output terminal, wherein the output terminal of the startup network is electrically connected to the input terminal of the voltage divider; a self-biasing network (334, 350, 354, 344) having a positive supply terminal (positive terminal of 334), a common terminal (ground), and an output terminal (output of 354), wherein the positive supply terminal of the Self-biasing network is electrically connected to the output terminal of the startup network, and wherein the common terminal of the self-biasing network is electrically connected to the common terminal of the voltage divider.

As to claim 8, figure 3 shows that the transistor is a PMOS transistor.

As to claim 11, figure 3 shows that the bandgap voltage reference generator also comprises a bias terminal, and wherein the output terminal of the self-biasing network is electrically connected to the bias terminal of the bandgap voltage reference generator.

As to claim 13, figure 3 it is inherent that the bandgap reference voltage generator further comprises ; positive supply terminal an; a common terminal, and wherein the operational amplifier also comprises a positive supply terminal and a common terminal, and wherein the positive supply terminal of the bandgap reference voltage generator is electrically connected to the positive supply terminal of said operational amplifier, and the common terminal of said bandgap reference voltage generator is electrically connected to the common terminal of the operational amplifier *(the circuits must be coupled between power supply and ground in order to operate as described in the specification).*

As to claim 14, figure 3 shows the common terminal of the voltage divider is electrically connected to the common terminal of the operational amplifier *(the operational amplifier must be connected to ground in order to operate properly).*

As to claim 15, figure 3 shows that the positive supply terminal of the startup network is electrically connected to the positive supply terminal of the operational amplifier *(the amplifier is must be connected to Vcc in order to operate properly).*

As to claim 16, figure 3 shows that the source terminal of the transistor is electrically connected to the positive supply terminal of the operational amplifier.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mosinskis et al. (USP 6529563) in view of Connell et al. (USP 6441594).

As to claim 17, Mosinskis et al.'s figure 3 shows all limitations of the claim except for a capacitor coupled between the output of the bandgap reference generator and ground. However, Connell et al.'s figure 2 teaches using a capacitor 126 coupled between the output of a reference voltage generator and ground for the purpose of stabilizing the output voltage. Therefore, it would have been obvious to one having ordinary skill in the art to add capacitors respectively coupled to the output of each voltage generator, i.e. the output of the bandgap reference voltage generator, the output of voltage generator (316, M1), and the output of the voltage divider (324, 326) in Mosinskis et al.'s figure 3 for the purpose of stabilizing the output voltage of each voltage generator in figure 3.

As to claim 18, the modified Mosinskis et al.'s figure 3 shows a capacitor coupled between the output of the voltage generator (M1, 316) and ground.

As to claim 19, the modified Mosinskis et al.'s figure 3 shows a capacitor coupled between the output of the output of the voltage divider and ground.

Allowable Subject Matter

5. Claims 12 and 20 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 12 would be allowable because the prior art fails to teach or suggest that the operational amplifier comprises a bias terminal, and wherein said output terminal of said self-biasing network is electrically connected to the bias terminal of the operational amplifier.

Claim 20 would be allowable because the prior art fails to teach or suggest a capacitor coupled between the output of the self-biasing network and the common terminal.

(10) Response to Argument

Appellant argues that "The office's interpretation is in direct conflict with the usage of the term as used in both Mosinskis and the present specification, which consistently use the term to mean shorted, at the same potential, or connected by a non-resistive connection". The Examiner respectfully disagrees. The present specification does not supply an explicit definition for the term "electrically connected". In addition, the use of the phase "electrically connected" to define a connection with intervening element is well known in the art, i.e. Fujiwara, USP 5229706, figure 2 and col. 4, lines 20-22 and lines 35-37, teaches that transistor TR1 is electrically connected to transistor TR2 via a resistor, and transistor TR3 is electrically connected to transistor TR4 via resistor R4; Tateishi, USP 5262688, figure 1 and col. 4, lines 1-4, teaches

that transistor 14 is electrically connected to power supply Vcc via current source 15; and Shao et al., USP 6154057, figure 2 and col. 2, lines 65-67, teaches that transistor 210 is electrically connected to voltage source V1 via resistor 206. Thus, a broad reasonable interpretation of the positive input terminal of Mosinskis et al.'s amplifier 334 is that it is electrically connected to the output terminal of the startup network (M3, R5) via resistor R3.

Appellant further argues that "The office's interpretation of the term electrically connected is in direct conflict with the usage of that term as used by those of ordinary skill in the art at the time the invention was made". The Examiner respectfully disagrees. As shown in the prior art noted above, the phase "electrically connected" to define a connection that include intervening element is used in the art. Therefore, the interpretation of the term "electrically connected" is not in conflict with the normal usage of that term by those of ordinary skill in the art at the time that the invention was made.

Appellant further argues that "The office interpretation of the term "electrically connected" renders the verbal description of circuit connectivity meaningless". The Examiner respectfully disagrees. The above examples demonstrate that "electrically connected" can be a connection via an intervening element. Therefore, it is not meaningless by interpreting the term "electrically connected" as connection via intervening element.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

Mosinskis et al.'s figure 3 and the modified Mosinskis et al.'s figure 3 anticipate the claims limitations. Therefore, it is believed that the rejections should be sustained.

Respectfully submitted,

Conferees:

Tim Callahan

Georgia Epps

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